Using Stencil: Design to Reduce SMT Defects

Solder paste printing is known as the root cause behind assembly defects. Because yield accounts for much of the margin, the greatest opportunity to improve profits can be gleaned by eradicating solder defects. This article examines some process adjustments made through stencil design and scaling that lead to assembly-defect reductions.

By Paul Lotosky, Michael Murphy, Robert Pearson, and Michael Tesch

Solder paste printing is understood to be the leading contributor of defects in the electronics assembly process. Because yield accounts for such a large percentage of the margin, the greatest opportunity to improve profitability in the assembly of most electronics can be gained by reducing or eliminating solder defects. This article examines process adjustments made through stencil design that correct a misalignment situation between the PCB and stencil, leading to a 43% reduction in assembly defects. Examples of each are found in Table 1.

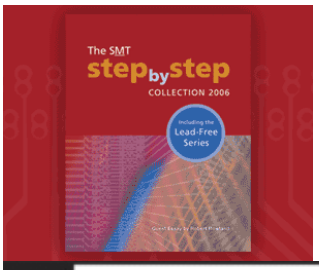

TABLE 1

Manufacturing Variables	Design Variables
Mis-registration of stencil aperture and pad due to PCB stretch and shrinkage	Incorrect stencil thickness
Mis-registration of stencil aperture and pad due to stencil image stretch and shrinkage	Improper aperture sizes or shapes
Poor PCB support	Poor gasketing due to raised features on the PCB surface (i.e. legend ink, vias, etc.)
Mis-registration of stencil aperture and pad due to printer alignment system or error	Inappropriate clearance in the component layout on the PCB

The main objective of the solder paste application process is to deposit the proper volume of solder paste consistently in the proper location. There are several factors that can impact an assembler's ability to do this. These factors fall into two categories: manufacturing variables and design variables. Alone or combined, these are the main causes of nearly all printing defects.

Historically, most companies have changed stencil designs to solve print-related defects. This approach, combined with the self-correcting nature of tin/lead solder pastes during reflow, helped enough to see acceptable results. But as companies have moved to less-forgiving lead-free solder pastes, and have increased the number and distribution of fine-featured components across their boards, it has become imperative that they uncover and correct the manufacturing variable that is the real source of the problem.

All tooling machinery has manufacturing tolerances. Machines used to produce PCBs and stencils are no exception. Generally, PCB and stencil suppliers will publish manufacturing tolerances. These tolerances are, in many cases, a restatement of figures that the maker of the critical piece of equipment that most influences the precision of the final PCB or stencil provides. Better-informed suppliers will base published tolerances on data that is collected as part of ongoing quality monitoring. One of the most significant contributors to printing defects caused by manufacturing variables is the misalignment of the stencil aperture to the corresponding pad on the PCB. The problem is that this occurs even though the PCB and stencil are within their published tolerances. Both are made from the same design data file; however, when made, the PCB could be on the low end of its manufactured tolerance, while the stencil is on the high end. This results in poor alignment on part or all of the board.

The scenario is a typical SMT assembly process used to manufacture engine-control modules. The only difference from a typical electronic assembly is that the substrate is a 0.007"-thick, flexible FR-4 board laminated onto a 0.080"-thick aluminum rigidizer.

Although there are more than 4,200 different component types on this assembly, including QFPs, SOICs, BGAs, capacitors, resistors, and connectors, a Pareto analysis of the defects revealed three specific components experienced high post-print defects for insufficient solder and solder shorts. These three components were located at the extreme ends of the board. Defects, as defined by percent of assembled units, are listed in Table 2.

TABLE 2

X-ray Defect Rates (Percent of Units Assembled)

Component	ID	Pitch	Excess Solder Before/After Scaling	Insufficient Solder Before/After Scaling	Total
A	SOIC	0.025"	0.16/0	0.10/0.08	0.26/0.08
B	QFP	0.025"	1.35/0.64	0.64/0.38	1.99/1.02
C	QFP	0.020"	1.45/0.65	0.82/0.79	2.27/1.44

* Data collected over three weeks on more than 125,000 units.

In addition to defects being identified by the post-reflow X-ray analysis, defects also were flagged at the printer due to solder paste off-pad printing detected by 2-D inspection - leading to a loss of productivity at the printer as stencil alignment was being adjusted to correct printing errors.

Previously, this issue did not affect production because Component A was a 0.040"-pitch part that could tolerate paste misalignment (Table 2). Due to a component design change, the pitch of Component A was reduced to 0.025", increasing the criticality of proper paste deposition. Prior to the design change with Component A, Component C received the most attention, as it was the finest-pitch component on the board. Component C also had the highest related defects - shorts and insufficients.

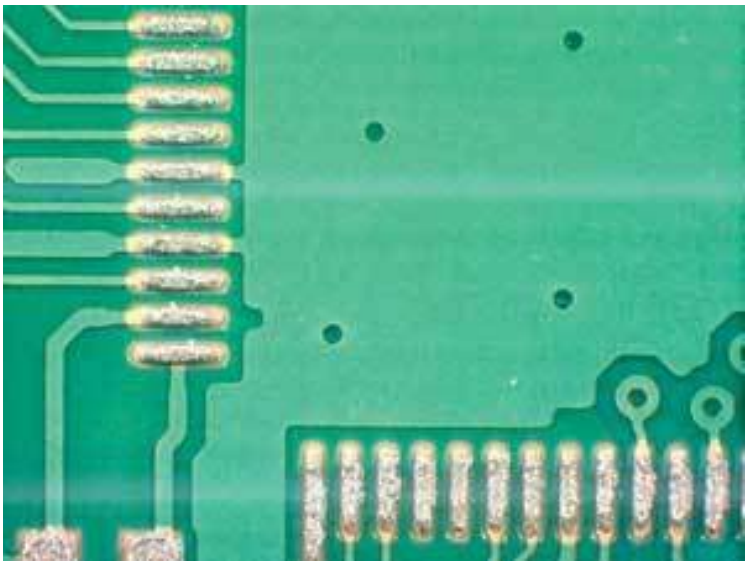

Figure 1. *Aligned paste deposited in Component C.*

When the stencil was aligned with the PCB for Component C, which yielded paste deposits deemed acceptable (Figure 1), the initial investigation revealed that the print deposits were not aligned properly on Component A pads (Figure 2). There was an offset in the X- and Y-axes that would not allow Components A and C to align properly - resulting in a compromise in the registration of the PCB and stencil. This was determined to be the cause of a high number of defects detected at X-ray of solder shorts and insufficients (Figure 3).

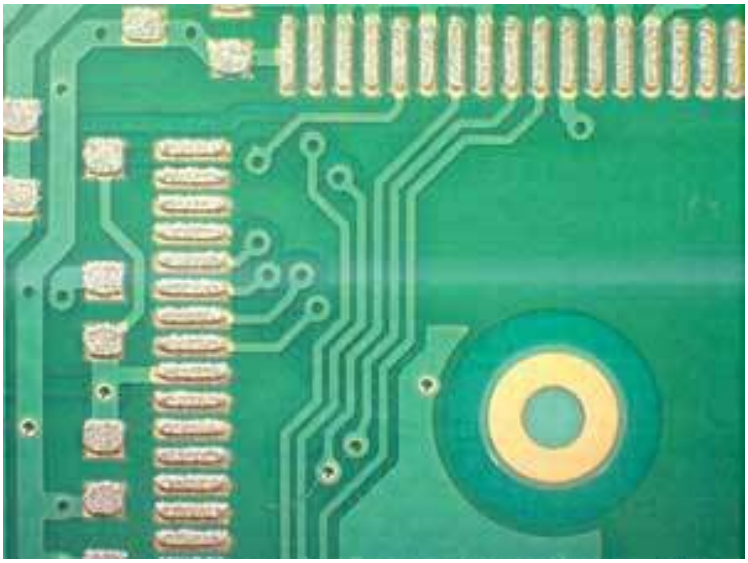

Figure 2. *Misaligned paste deposits on Component A.*

Printer settings were optimized for X, Y, and Theta alignments; however, print deposits were not aligning with the pads. An investigation into the stencil Gerber file was conducted to verify that stencil-aperture design and locations were correct. As part of the investigation to verify that the stencil was manufactured properly, the stencil was measured on an automated CAD system, and found to be within specification.

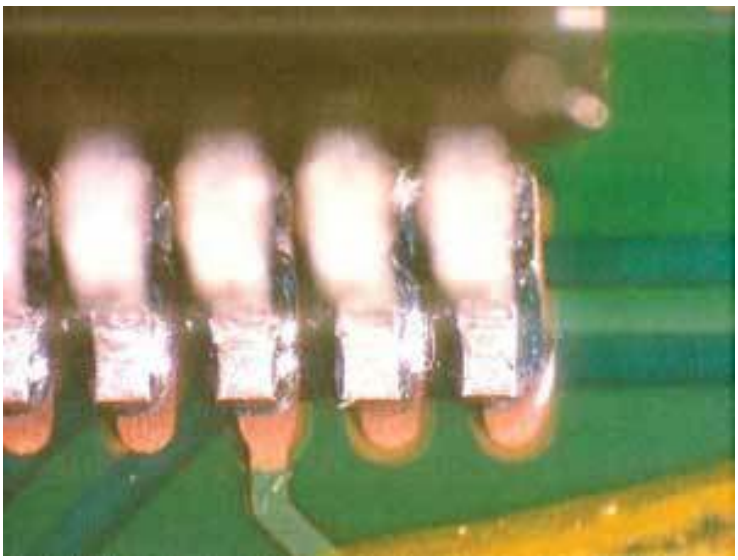

Figure 3. *Component A - insufficient solder paste after reflow.*

Because the stencil and Gerber files matched, the next step was to investigate incoming boards. These particular substrates are processed in-house by laminating a 0.007" FR-4 flexible circuit onto a 0.080"-thick aluminum rigidizer. In-house process steps were:

1. Place rigidizer on step-up table;
2. Place solid-film Pressure Sensitive Adhesive (PSA) onto rigidizer;
3. Place FR-4 onto PSA;
4. Pressurize;
5. Cure final laminate.

Board measurements were conducted using a coordinate-measurement machine to verify board dimensions upon entry, after lamination, and after cure. Using six reference points (Figure 4), measurements were made from one origin point to six reference points across the board. Thirty replicate samples were taken for each point.

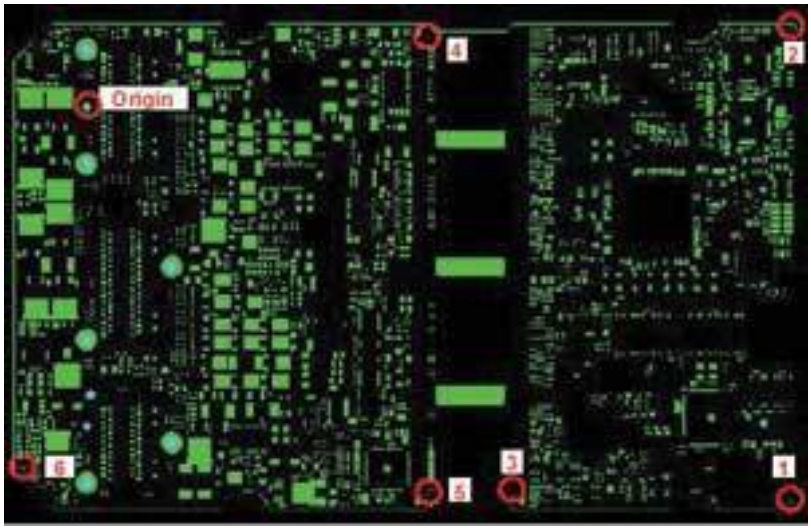

Figure 4. *Origin and reference measurement points.*

Normal probability charts of non-laminated circuits, laminated pre-bake assemblies, and post-bake assemblies demonstrated normal distribution. The null hypothesis is that the data set is normal. P-values are all greater than 0.0; therefore, the data set is from a normal distribution. When testing for equal variance of non-laminated circuits, laminated pre-bake assemblies, and post-bake assemblies, the null hypothesis is that the two data sets have equal variance. The p-value is greater than 0.05. From this, we conclude that there is no significant difference between the variance of the two data sets.

Analysis on the tests for equal variance revealed in-process steps were not factors in deviations of board dimensions. The team also performed a two-sample T-test using the mean statistic of each data set. The two-sample T-test analysis supported equal-variance test conclusions showing no significant difference between each data set. Based on normal probability plots and tests for equal-variance analysis, it was determined that in-process steps were not factors in deviations of board dimensions. Analysis of board measurements revealed that the boards were within specification; however, they were significantly different from the Gerber files used to manufacture the boards and subsequent stencils. In fact, the boards were reduced by about 0.0005" per board inch in the X and Y direction.

Short-term Corrective Action

While depleting current board inventory and meeting production requirements, the most feasible solution to reduce defects was to partner with the stencil supplier to match the stencil to the PCB. The challenge was to produce a stencil that compensated for board shrinkage. In other words, have a stencil made to the PCB, not to the Gerber data. The first step was to validate the offset in board dimensions. One company* used PCB automated board-measuring equipment to verify that the 0.0005" per-board offset was correct. Then they used features built into automated stencil ordering, design, and configuration software** to enter offset data and generate a modified Gerber file to produce the new stencil. This data-scaling functionality is shown in Figures 5 and 6.

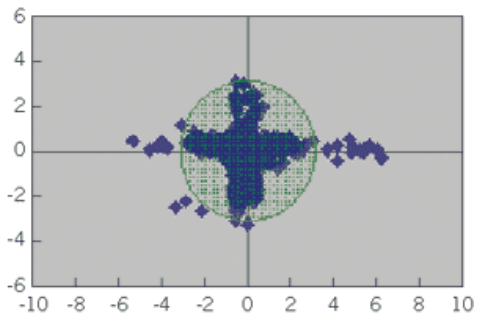

Figure 5. *Pad positional deviation measurements (mils) between a stencil and PCB prior to scaling. Relative to the original Gerber data, some pads were off by as much as 0.005”-0.006”.*

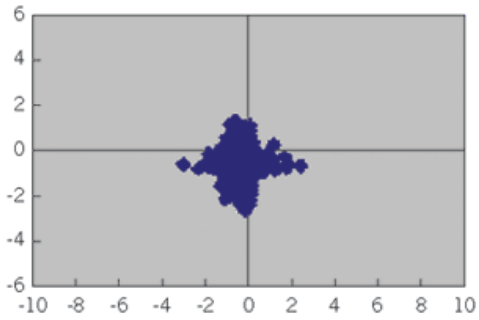

Figure 6. *The same X, Y pad aperture deviation after scaling the stencil to the PCB.*

New stencils were placed in production where improvements were noticed immediately in the pass rate for 2-D inspection. Prints were centered in X and Y directions. With print deposits aligned across the circuit, 2-D inspection at the printer was not rejecting prints. The test was to see the effect on first-time yield at X-ray. Total defects for excessive solder and insufficients were reduced by an average of 43%, with the greatest reduction (69%) on Component A.

Conclusion

When looking to reduce printing defects, tolerances between PCBs and SMT processes must be considered. By scaling the stencil to the PCB, registration problems between PCBs and stencils can be reduced. This can reduce or eliminate defects and increase yield and profitability.

* Cookson Electronics. ** Alpha Dimensions, Cookson Electronics.

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